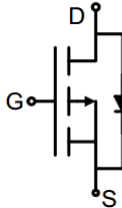
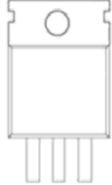



P-Channel Enhancement Mode Power MOSFET

Description <p>The G30P10T uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.</p>		 Schematic diagram	
General Features <ul style="list-style-type: none"> ● V_{DS} -100V ● I_D (at $V_{GS} = -10V$) -41A ● $R_{DS(ON)}$ (at $V_{GS} = -10V$) < 37mΩ ● 100% Avalanche Tested ● RoHS Compliant 		 Marking and pin assignment	
Application <ul style="list-style-type: none"> ● Power switch ● DC/DC converters 		 TO-220	
Device	Package	Marking	Packaging
G30P10T	TO-220	G30P10	50pcs/Tube

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-100	V
Continuous Drain Current	I_D	-41	A
Pulsed Drain Current (note1)	I_{DM}	-160	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	123	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	$^\circ\text{C}$

Thermal Resistance

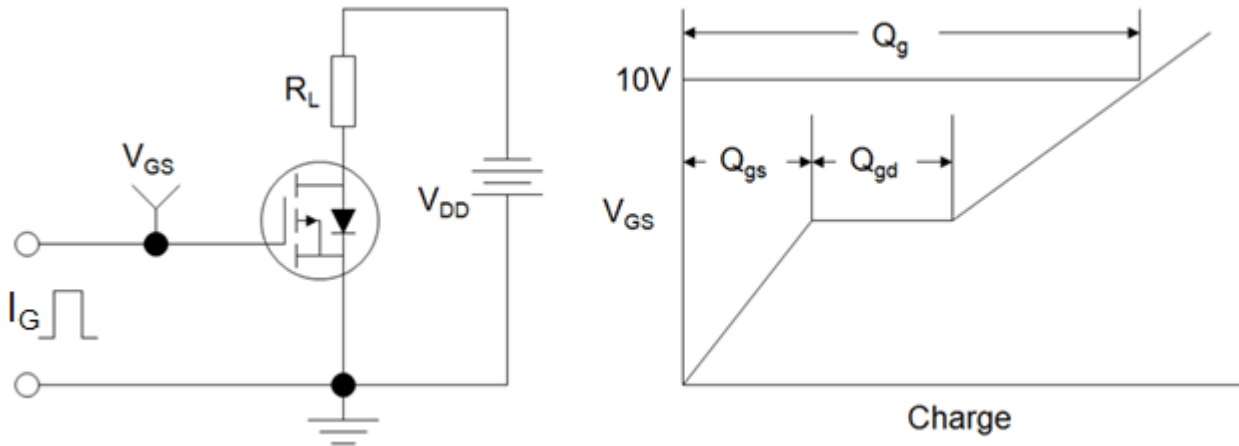
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (note3)	R_{thJC}	1.01	$^\circ\text{C/W}$

Specifications $T_J = 25^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100V, V_{GS} = 0V$	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.5	-2	-2.5	V
Drain-Source On-Resistance (note2)	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -22A$	--	31	37	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = -5V, I_D = -22A$	--	60	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = -50V,$ $f = 1.0\text{MHz}$	--	5612	--	pF
Output Capacitance	C_{oss}		--	180	--	
Reverse Transfer Capacitance	C_{rss}		--	80	--	
Total Gate Charge	Q_g	$V_{DD} = -50V,$ $I_D = -22A,$ $V_{GS} = -10V$	--	102	--	nC
Gate-Source Charge	Q_{gs}		--	25	--	
Gate-Drain Charge	Q_{gd}		--	19	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -50V,$ $I_D = -22A,$ $R_G = 2.7\Omega$	--	15	--	ns
Turn-on Rise Time	t_r		--	38	--	
Turn-off Delay Time	$t_{d(off)}$		--	86	--	
Turn-off Fall Time	t_f		--	68	--	
Drain-Source Body Diode Characteristics						
Body Diode Voltage (note2)	V_{SD}	$I_S = -22A, V_{GS} = 0V$	--	--	-1.3	V
Reverse Recovery Time	T_{rr}	$I_S = -22A, V_{GS} = 0V$ $di/dt = -100A/\mu s$	--	36	--	nS
Reverse Recovery Charge	Q_{rr}		--	62	--	nC

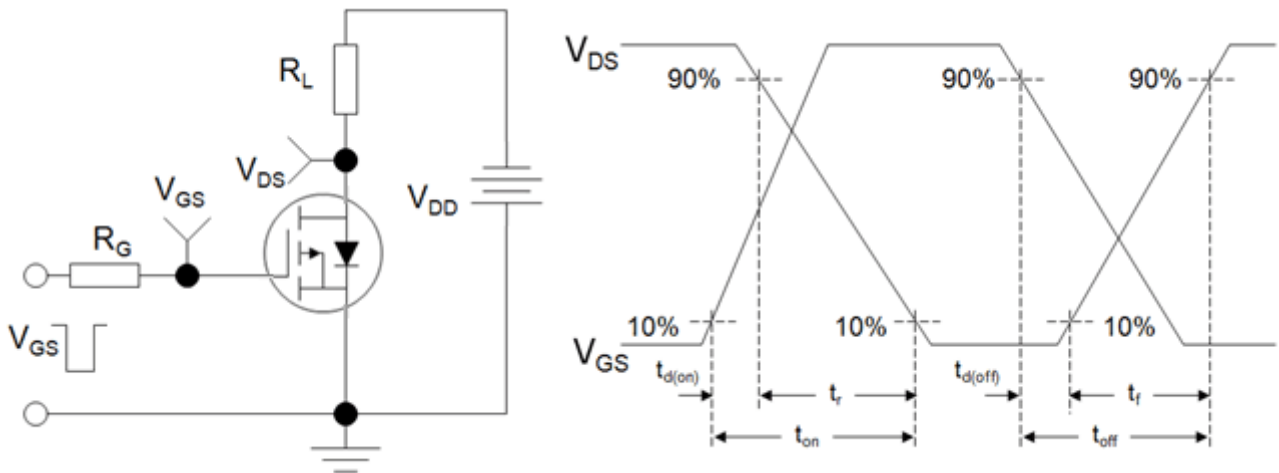
Notes

- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in² copper pad of FR4 board

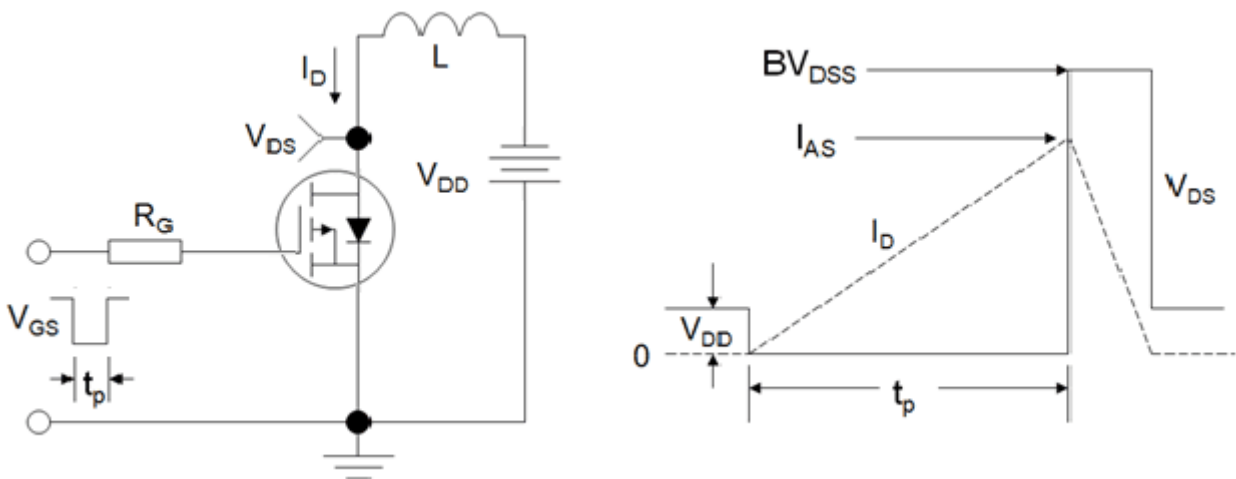
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

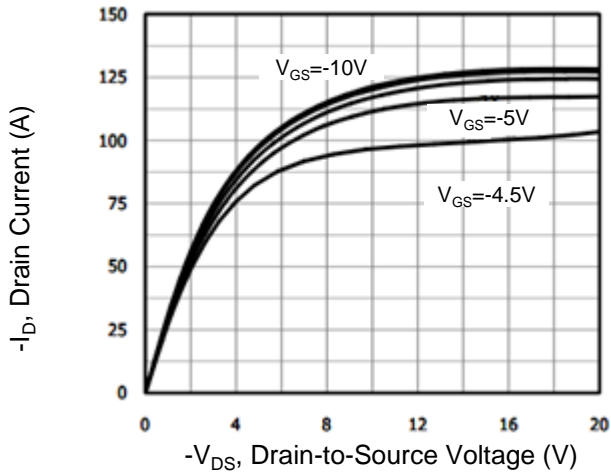


Figure 2. Transfer Characteristics

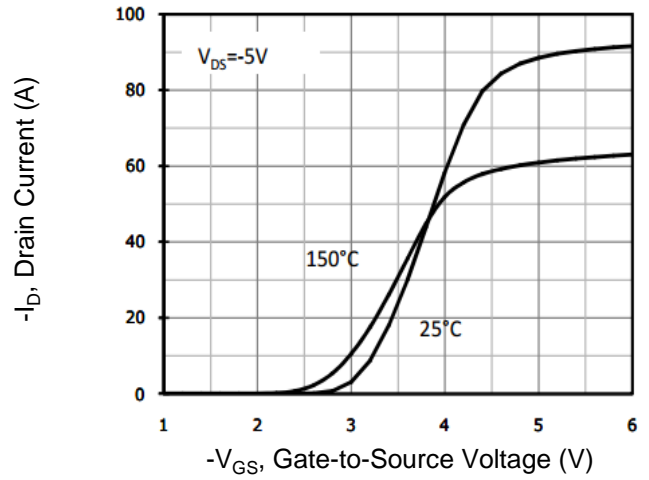


Figure 3. Drain Source On Resistance

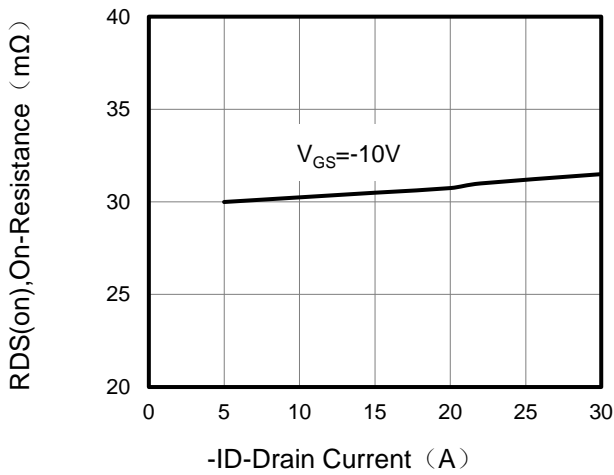


Figure 4. Gate Charge

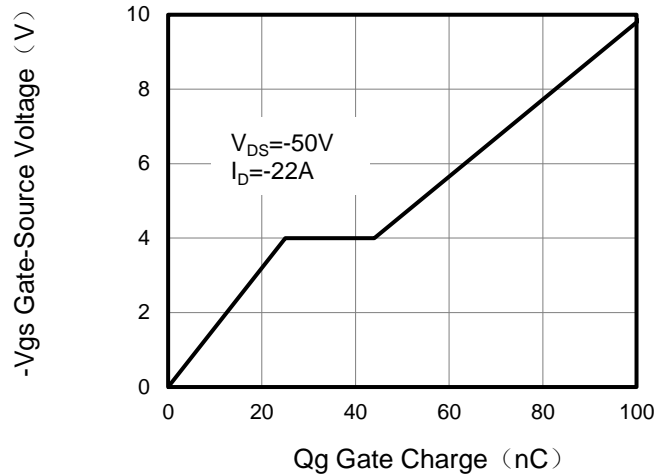


Figure 5. Capacitance vs Vds

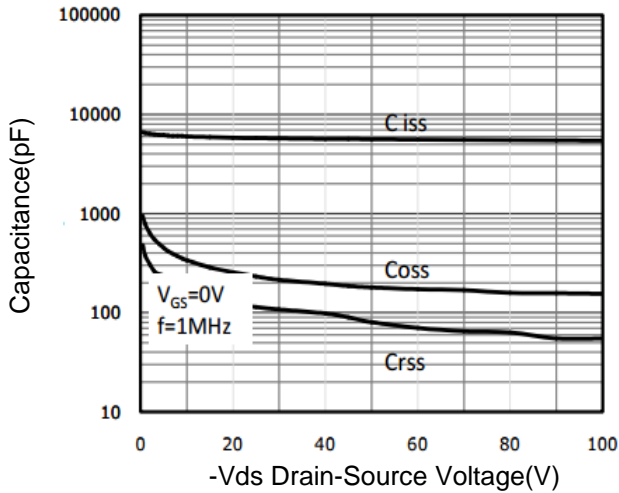
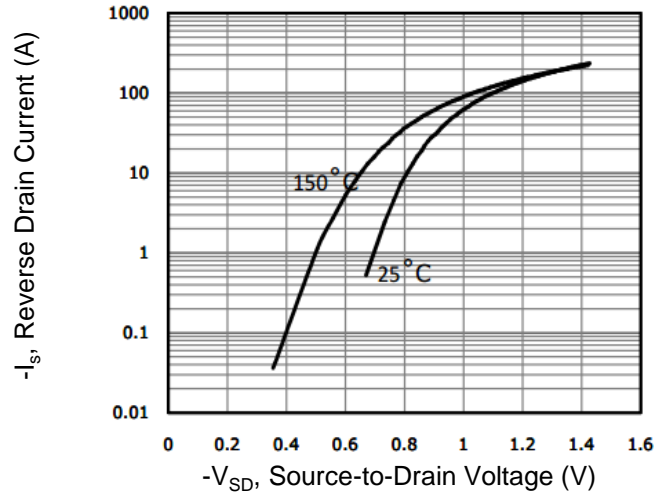


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

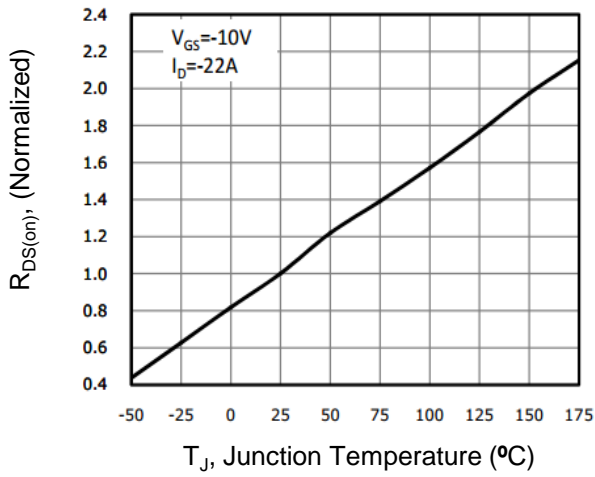


Figure 8. Safe Operation Area

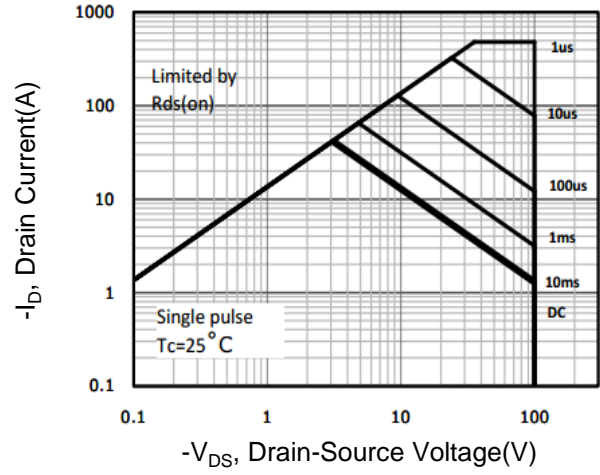
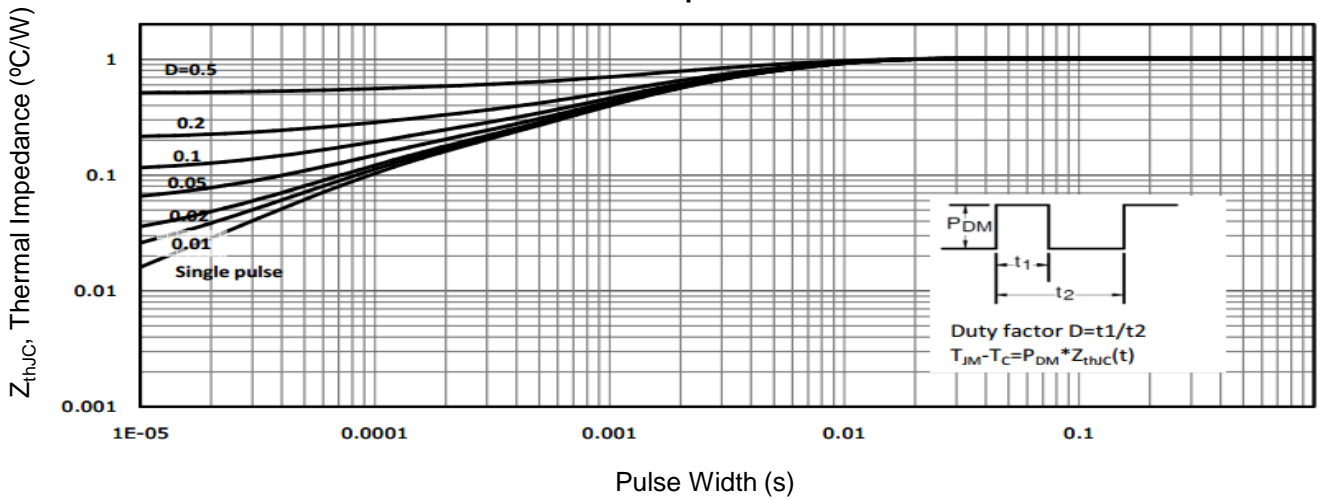
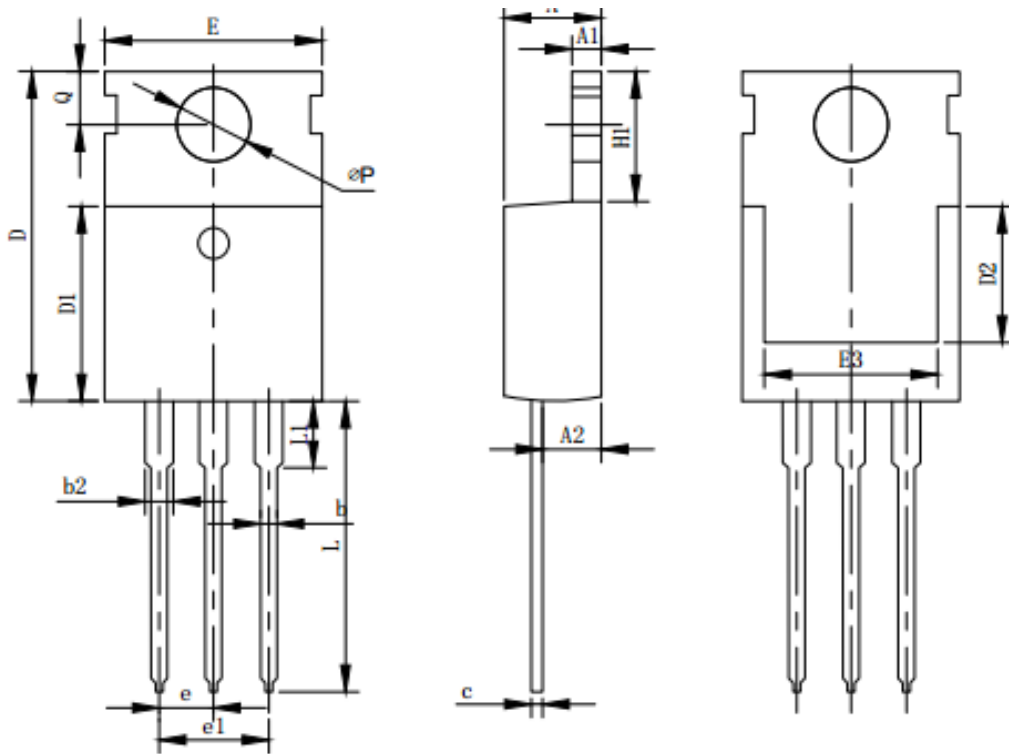


Figure 9. Normalized Maximum Transient Thermal Impedance



TO-220 Package Information



Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	4.37	4.57	4.7
A1	1.25	1.3	1.4
A2	2.2	2.4	2.6
b	0.7	0.8	0.95
b2	1.7	1.27	1.47
c	0.45	0.5	0.6
D	15.1	15.6	16.1
D1	8.8	9.1	9.4
D2	5.5		
E	9.7	10	10.3
e	2.54BSC		
e1	5.08BSC		
H1	6.25	6.5	6.85
L	12.75	13.5	13.8
L1		3.1	3.4
øP	3.4	3.6	3.8
Q	2.6	2.8	3